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(54) Heterojunction bipolar transistor and optical waveguide device for monolithic integration

(57) A method for forming a monolithic integrated structure including a heterojunction bipolar transistor and an optical waveguide device which method comprises forming on a substrate (14) a plurality of successive epitaxial semiconductor layers, said layers being selectively etched to provide on said substrate a first structure of said transistor and a second structure of said waveguide device.

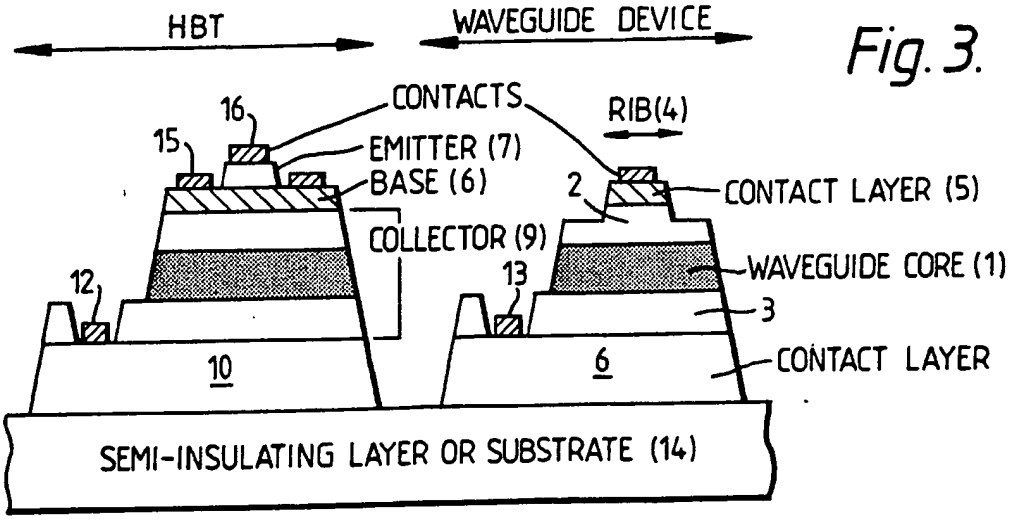

Fig. 3.

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.
The print reflects an assignment of the application under the provisions of Section 30 of the Patents Act 1977.

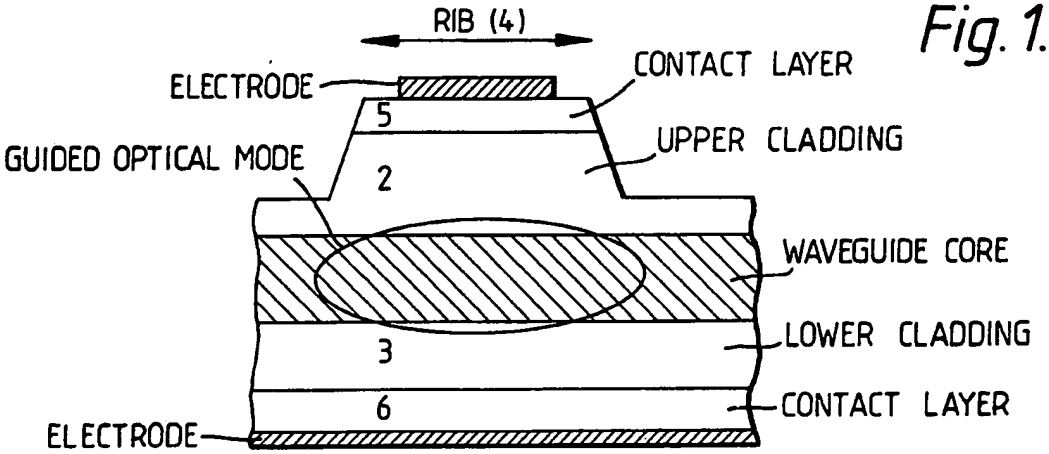

Fig. 1.

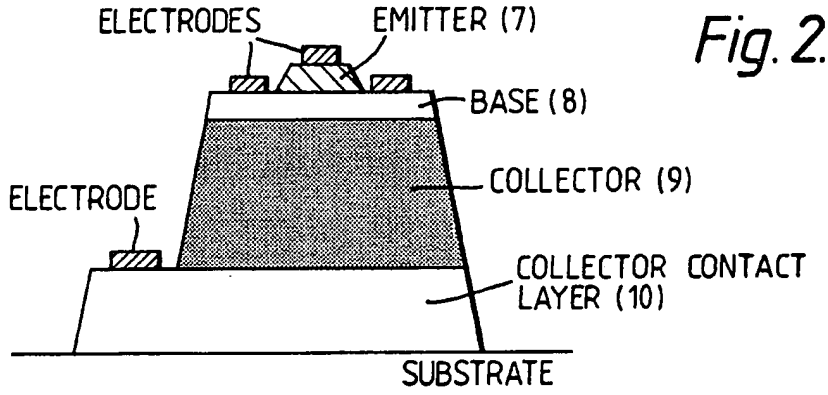

Fig. 2.

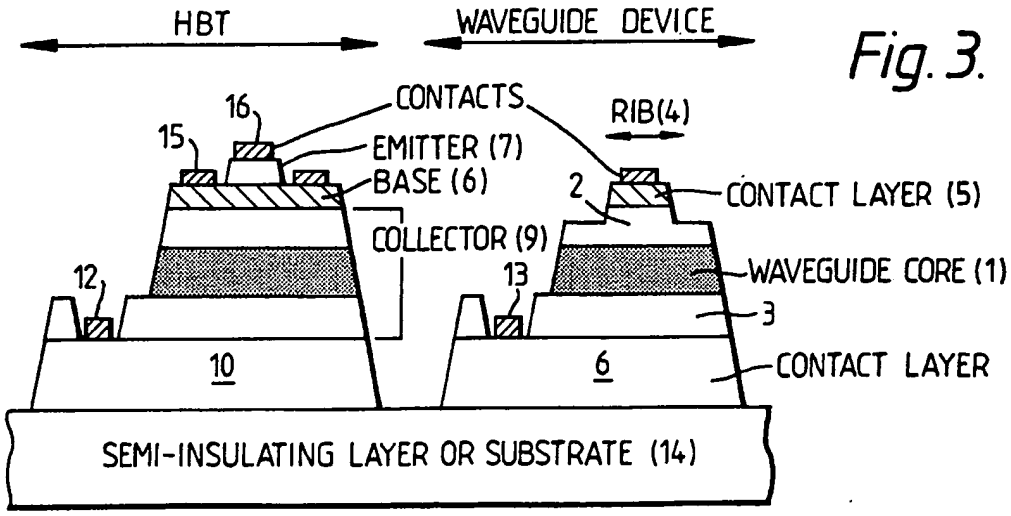

Fig. 3.

HETEROJUNCTION BIPOLAR TRANSISTOR AND OPTICAL WAVEGUIDE DEVICE FOR MONOLITHIC INTEGRATION

The invention relates to a method of forming a monolithic integrated structure including a hetrojunction bipolar transistor and an optical waveguide device.

The drive voltages required by optical switches and modulators are typically higher than standard electronic logic levels, so external drive circuits are normally required. The ability to place the drive circuit for the switch on the same chip as the switch itself permits interfacing to be achieved at standard electronic logic levels, thus avoiding the need for external buffer amplification. Furthermore the close proximity of the switch and its drive transistor is highly advantageous in high speed designs. The ability to monolithically integrate the optical waveguide devices with complex electronic circuits such as amplifiers and logic gates further extends the capability of the optoelectronic integrated circuit; for example self-routing and self-biasing functions may be realised within a monolithic optical switch component. As in other areas of electronics, monolithic integration of the separate functions should yield improvements in cost, reliability and functionality.

Previously published work has demonstrated a transistor and a simple on/off modulator combined in a single device (Y.Okada et al "Fabrication of double graded hetrojunction bipolar transistor waveguide structure optical intensity modulator" Proc. I00C89, Kobe, Japan). Combining the functions in this way limits the flexibility severely: more complex electronic functions (e.g. logic circuits) cannot

easily be included in such a scheme. Further more the above publication does not describe the integration of alternative optical waveguide device functions such as a four-port optical switch.

The discrete optical waveguide devices and HBT circuits described to date are based on mutually incompatible semiconductor structures. To integrate such devices monolithically would demand repeated epitaxial growth processes during device fabrication, which would complicate the processing considerably and make high yield and reliability more difficult to achieve. In the present invention the electronic and optical devices share a common epitaxial layer structure requiring only a single growth step. This major advantage has been achieved without significant compromise in the performance either of the optical device or of the HBT.

According to the invention that is provided a method of forming a monolithic integrated structure including a hetrojunction bipolar transistor and an optical waveguide device which method comprises forming on a substrate a plurality of successive epitaxial semiconductor layers, said layers being selectively etched to provide on said substrate a first structure of said transistor and a second structure of said waveguide device.

In one embodiment of the present invention the purality of layers include first, second, third, fourth and fifth epitaxial layers, said third layer providing a waveguide core layer of the waveguide device, said second and fourth layers providing lower and upper cladding layers for the core layer, the cladding layers being of a lower refractive indent than the core layer and said first and third layers providing contact layers of the waveguide device. The etching

of said layers include etching a rib into the fourth and fifth layers of said waveguide device. The second, third and fourth epitaxial layers provide a collector for said transistor, said fifth epitaxial layer provides a base of said transistor and said first epitaxial layer provides a contact layer for the transistor, an emitter is provided on said base of the transistor. The fifth layer has a doping opposite to the doping of the first, second, third and fourth layer.

Preferably said plurality of layers are formed of a material selected from InP, InGaAsP, InGaAs, InGaAlAs, GaAs and AlGaAs and said substrate is a layer of InP, GaAs or Si.

The structures for integrated optical switch/modulator elements and heterojunction bipolar transistors (HBTs) are particularly suitable for monolithic integration. Integrated structures of this type will be used in optical switching and signal processing systems in order to provide standard electronic logic level interfaces to the optical devices and for on-chip electronic processing related to the optical function. The novel design presented here needs only one epitaxial growth process, with the same semiconductor layer structure being employed for both the HBT and the optical waveguide device. The relative simplicity of the device structures should lead to reduced manufacturing costs for integrated HBT/optical waveguide devices and improved production yield, without major compromise in the performance of either the transistor or the optical device.

The invention will now be described further by way of example with reference to the accompanying drawings in which:-

Figure 1 illustrates a waveguide structure for modulator or switch;

Figure 2 illustrates a structure of hetrojunction bipolar transistor (HBT); and,

Figure 3 illustrates an integrated structure for HBT and optical waveguide device embodying the invention.

The general characteristics of the separate optical and electronic devices, which are to be integrated, are hereinafter considered with reference to figures 1 and 2.

The necessary layers to form an optical waveguide for the switch/modulator are, as shown schematically in figure 1, a high refractive index semiconductor layer forming the waveguide core 1 and upper 2 and lower 3 cladding layers of lower refractive index semiconductor. For the purpose of illustration a device operating at 1.3 or 1.55 μm wavelength might employ InP for layers 2 and 3 and an InGaAsP alloy with bandgap ≈1.15 μm for layer 1. The heterostructure provides the vertical confinement of the optical waveguide mode. Lateral confinement may be achieved by etching a rib 4 into the upper semiconductor layer. A p-doped layer 5 and an n-doped layer 6 permit a high electrical field to be established in the region encompassing the guided optical mode. A metal contact is formed on the surface of the p-layer 5, while in a discrete device the metal n-contact may be on the lower surface of the n-region 6. Alternatively a contact may be provided on the top surface of the layer 6 after local etching to reveal this layer, or elsewhere. The application of a reverse voltage to this PIN structure results in phase modulation of the optical wave via the electro-optic effect. Optical

intensity modulation and space switching functions are achieved by incorporating the above waveguide in well known integrated optical device structures such as the Mach-Zehnder interferometer and the directional coupler switch. The particular waveguide layouts needed for these functions are not essential to the present invention.

A typical structure for a heterojunction bipolar transistor is shown schematically in figure 2. The necessary layers are an emitter 7, base 8 and collector 9. A further layer 1 with appropriate doping may also be included for the collector contact. The central base layer has opposite doping with respect to that of the emitter and collector. In the example discussed here, the composition of this layer is chosen to provide a narrower (longer wavelength) band gap, which inhibits the injection of holes from the emitter layer into the base and thus improves the current gain. Electrical contact is provided to all three sections by established etching and metal deposition processes.

Referring to figure 3 which illustrates an embodiment of the present invention a plurality of successive epitaxial semiconductor layers (first, second, third, fourth and fifth) are formed on a substrate 14. These epitaxial layers are selectively etched to form a first structure of the HBT and a second structure of the waveguide device. The second, third and fourth epitaxial layers provide the collector layer 9 of the transistor and the waveguide core 1 with lower and upper cladding layers 2 and 3 of the waveguide device. The first epitaxial layer provides the contact layer 6 of the waveguide device and the collector contact layer 10 of the transistor. The fifth epitaxial layer provides the contact layer 5 of the

waveguide device and the base 8 of the transistor . The emitter layer 7 is formed on the base 8.

The embodiment of the invention illustrated with reference to figure 3, preferably employs device elements with the following characteristics in order to achieve compatibility with respect to semiconductor layer structures while maintaining satisfactory device performance:

- All of the layers within the optical waveguide structure have band gap wavelengths less than the operating wavelength of the switch, in order to minimise direct transitions giving rise to absorption of the optical wave.

- The guiding core 1 and cladding layers 2, 3 of the waveguide are formed with low doping levels to further reduce the optical absorption. The material forming the waveguide core layer 1 will have narrower band gap than that of the cladding: for example in a device for 1.3μm or 1.55μm operation the core may be of InGaAsP ($\lambda g \approx 1.15\mu m$) and the cladding may be InP. In the integrated structure these layers are incorporated into the collector region 9 of the transistor and are grown upon a highly doped n layer 10,6 to accommodate the electrical contacts 12,13.

- The entire structure is formed upon a substrate or layer 14 of semi-insulating semiconductor material, so that electrical isolation may be achieved as required by etching through the lower contact layer of both the transistor and the optical switch.

- The same material composition is employed for the transistor base region 8 and for the upper contact layer 5 of the optical switch. This layer has a narrower band gap than the immediately adjacent emitter and collector layers within the transistor structure. For example in a device based upon InP, a layer of the alloy InGaAsP ($\lambda g \approx 1.15\mu m$) may be employed. This layer may carry an appropriately high doping to facilitate its use as a contact layer; high transistor gain is maintained as a result of the blocking character of the heterojunction.

Electrical contacts 16, 15 and 12 to the emitter 7, base 8 and collector 9 of the transistor are achieved by etching a suitable profile to expose the layers and by the subsequent deposition of appropriate metallisation. Electrical contact to the n-doped lower layer of the switch 13 may be made in the same way as to the collector contact 12 of the transistor.

The validity of the approach described here has been verified by computer simulation and by experiments in which transistors and electro-optic directional coupler switches were fabricated using common specifications for the semiconductor layers forming the devices. Preliminary results indicate that the gain and the breakdown voltage of the transistor are sufficient to provide the driving voltage for the switch from standard electronic logic levels inputs. In particular breakdown voltage $>20V$ and gain >200 have been achieved in the transistor, along with an optical switch operating voltage of 20V.

CLAIMS:

1. A method of forming a monolithic integrated structure including a hetrojunction bipolar transistor and an optical waveguide device which method comprises forming on a substrate a plurality of successive epitaxial semiconductor layers, said layers being selectively etched to provide on said substrate a first structure of said transistor and a second structure of said waveguide device.

2. A method as claimed in claim 1, in which said plurality of layers include first, second, third, fourth and fifth epitaxial layers, said third layer providing a waveguide core layer of the waveguide device, said second and fourth layers providing lower and upper cladding layers for the core layer, the cladding layers being of a lower refractive index than the core layer and said first and third layers providing contact layers of the waveguide device.

3. A method as claimed in claim 2, in which said etching of said layers includes etching a rib into the fourth and fifth layers of said waveguide device.

4. A method as claimed in claim 2 or 3, in which said second, third and fourth epitaxial layers provide a collector for said transistor, said fifth epitaxial layer provides a base of said transistor and said first epitaxial layer provides a contact layer for the transistor, said method further comprising providing an emitter on said base of the transistor.

5. A method as claimed in any one of claims 2 to 4, in which said fifth layer has a doping opposite to the doping of the first, second third and fourth layer.

6. A method as claimed in any one of the preceding claims, in which said plurality of layers are formed of a material selected from InP, InGaAsP, InGaAs, InGaAlAs, GaAs and AlGaAs.

7. A method as claimed in any one of the preceding claims, in which said substrate is a layer of InP, GaAs or Si.

8. A method of forming a monolithic integrated structure substantially as hereinbefore described with reference to figure 3 of the accompanying drawings.

9. A monolithic integrated structure made by the method claimed in any one the of the preceding claims.

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